TRANSMITTAL OF FORMAL DRAWINGS

Docket No. 15184

In Re Application Of: SEPTA INDO

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PATENT & TRADEMARK OFFICE FEB 28 2002

Serial No.	Filing Date	Batch No.	Examiner	Art Unit
10/028,111	December 20, 2001	unassigned	unassigned	unassigned

Invention:

WATCHDOG TIMER AND METHOD FOR DETECTIING ABNORMAL OPERATION OF COMPUTER, AND COMPUTER INCLUDING THE TIMER

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Transmitted herewith are:

10 sheets of formal drawing(s) for this application.

Each sheet of drawing indicates the identifying indicia suggested in 37 CFR Section 1.84(c) on the reverse side of the drawing.

Signature

Dated: **January 24, 2002**

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Garden City, New York 11530

I certify that this document and attached formal drawings are being deposited on Jan 24, 2002 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

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Michelle Mustafa

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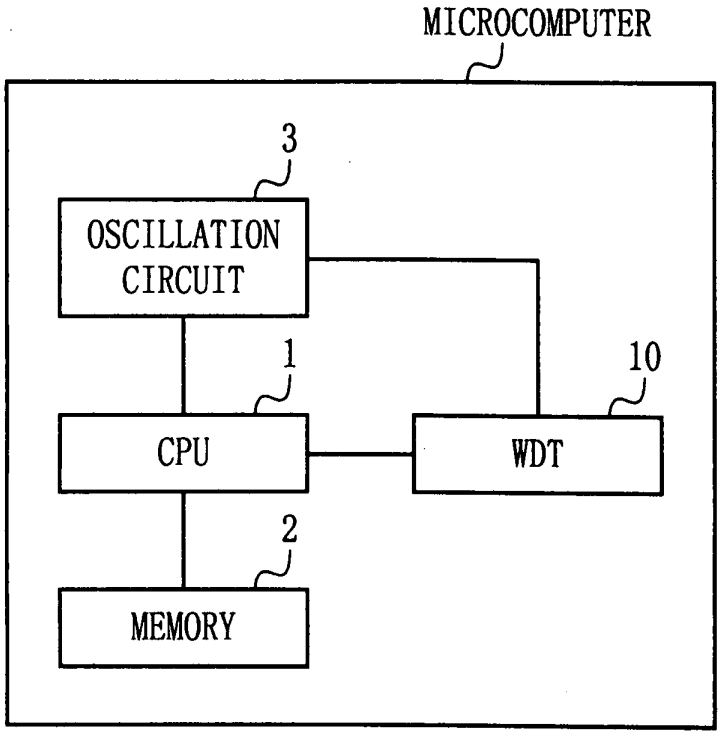

FIG. 1

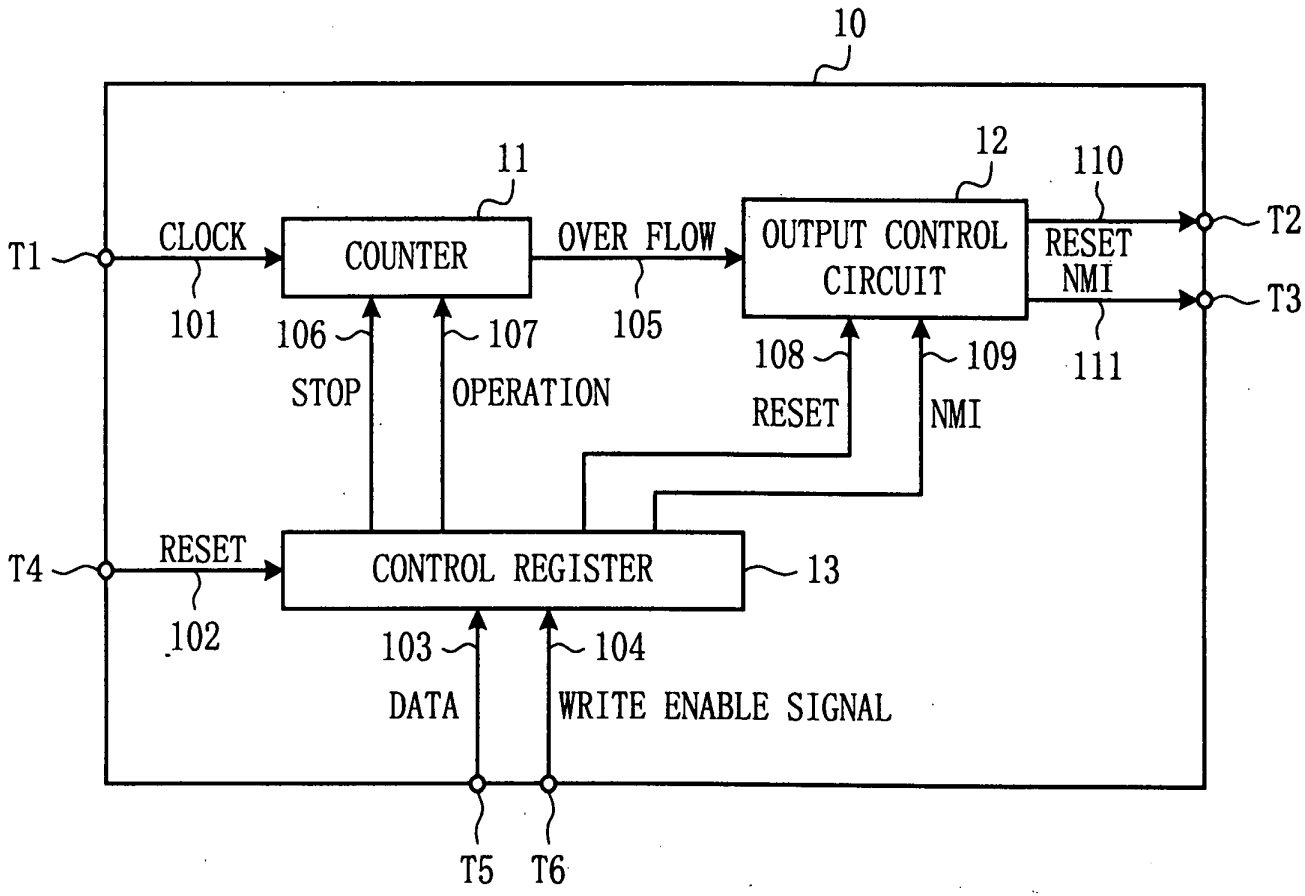
10
11
12
110
T1
CLOCK
COUNTER
OVER FLOW
OUTPUT CONTROL CIRCUIT
RESET
NMI
T2
T3
101
106
107
105
108
109
111
STOP
OPERATION
RESET
NMI
T4
RESET
CONTROL REGISTER
13
102
103
104
DATA
WRITE ENABLE SIGNAL
T5
T6

FIG. 2

FIG. 3A

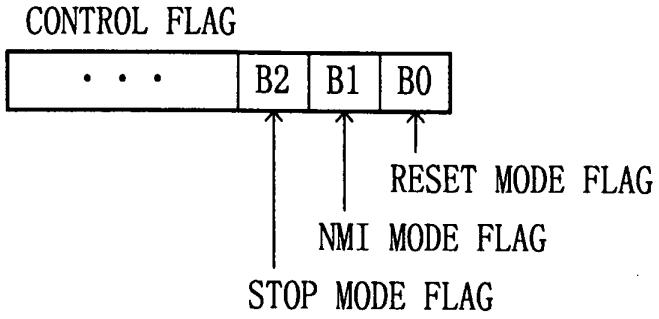

FIG. 3B

OPERATIONAL MODE	B2	B1	B0
RESET MODE	×	×	0
NMI MODE	×	0	1
STOP MODE	0	1	1

×:DON'T CARE

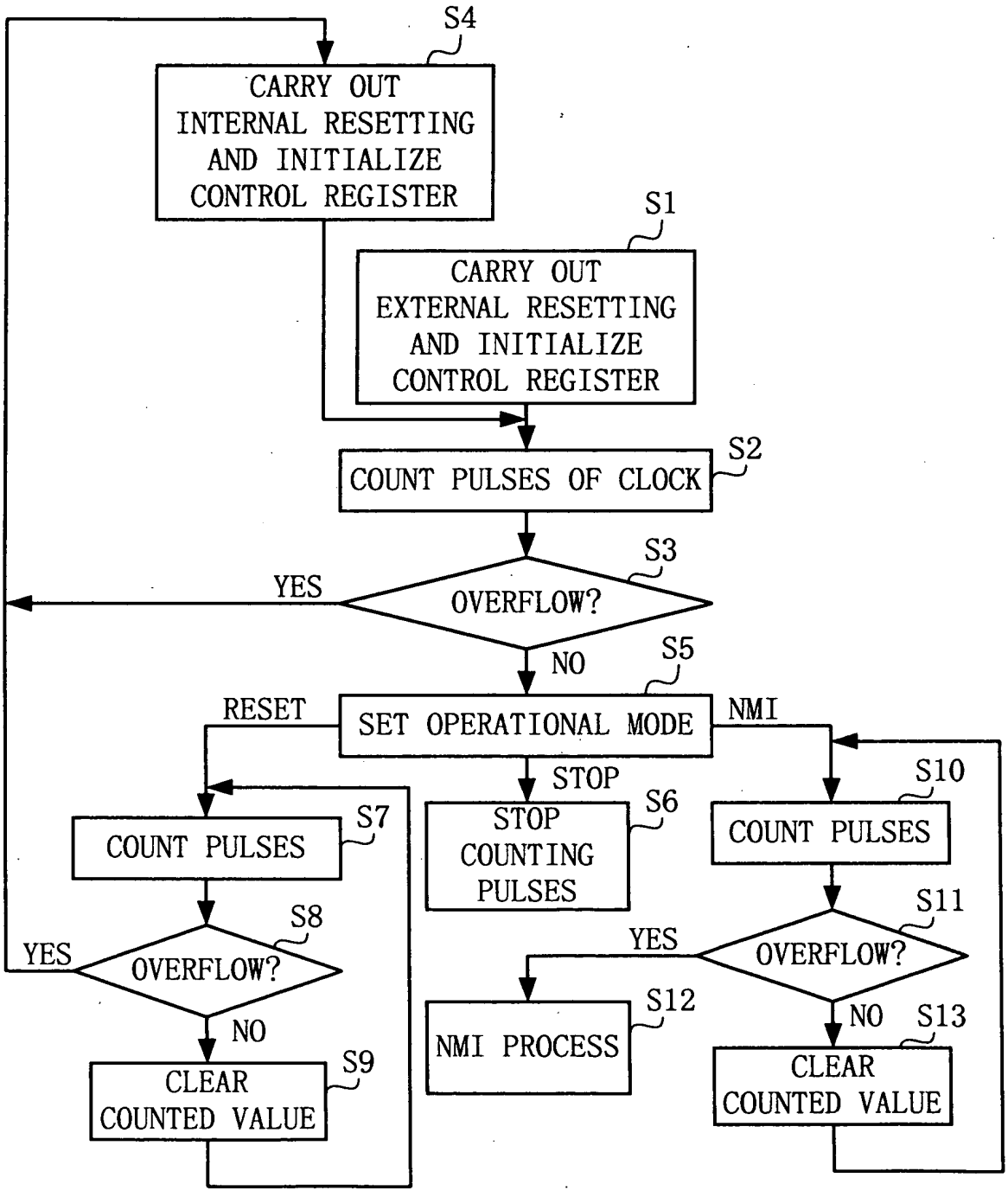
S4
CARRY OUT INTERNAL RESETTING AND INITIALIZE CONTROL REGISTER
S1
CARRY OUT EXTERNAL RESETTING AND INITIALIZE CONTROL REGISTER
S2
COUNT PULSES OF CLOCK
S3
OVERFLOW?
YES
NO
S5
SET OPERATIONAL MODE
RESET
STOP
NMI
S7
COUNT PULSES
S6
STOP COUNTING PULSES
S10
COUNT PULSES
S8
OVERFLOW?
YES
S11
OVERFLOW?
YES
NO
S9
CLEAR COUNTED VALUE
S12
NMI PROCESS
NO
S13
CLEAR COUNTED VALUE

FIG. 4

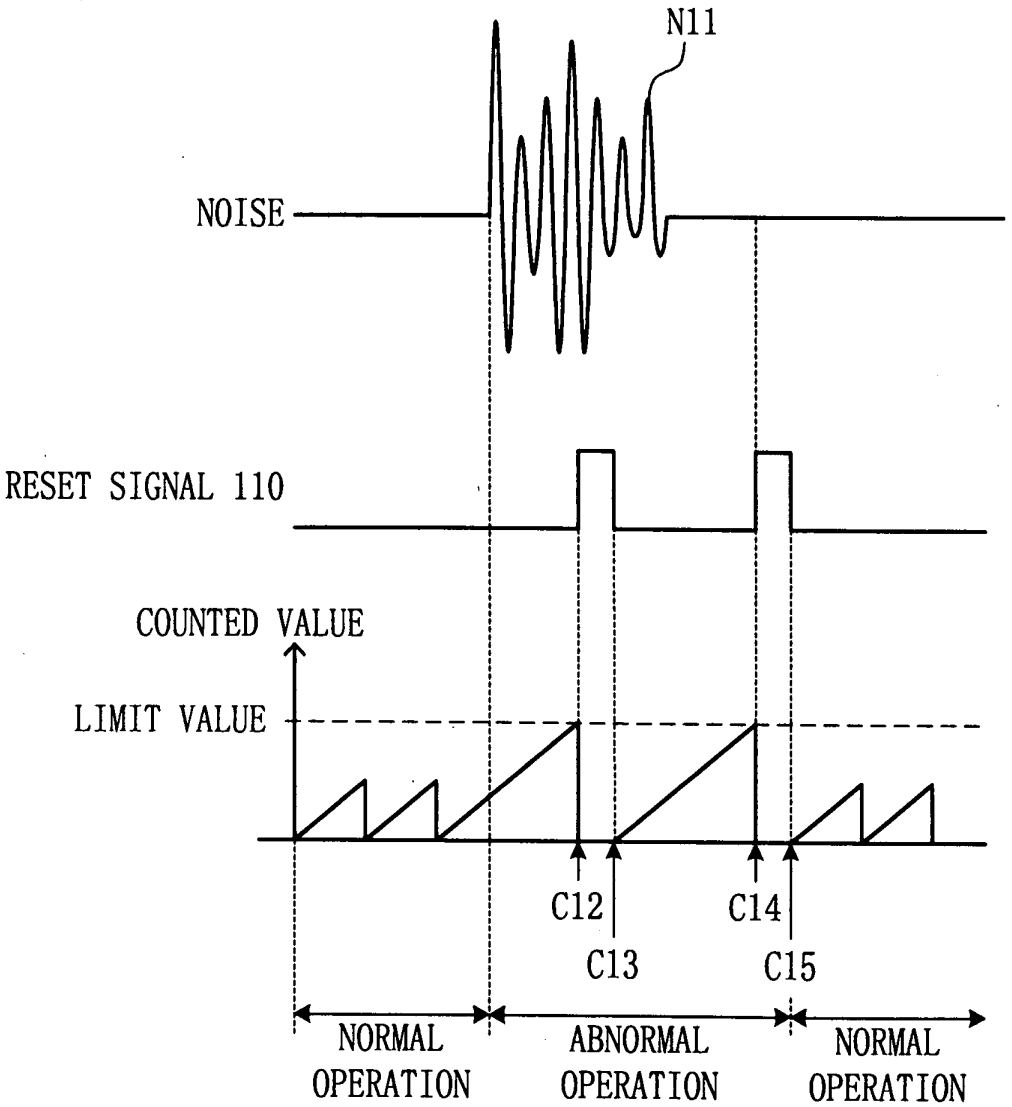
N11
NOISE
RESET SIGNAL 110
COUNTED VALUE
LIMIT VALUE
C12
C13
C14
C15
NORMAL OPERATION
ABNORMAL OPERATION
NORMAL OPERATION

FIG. 5

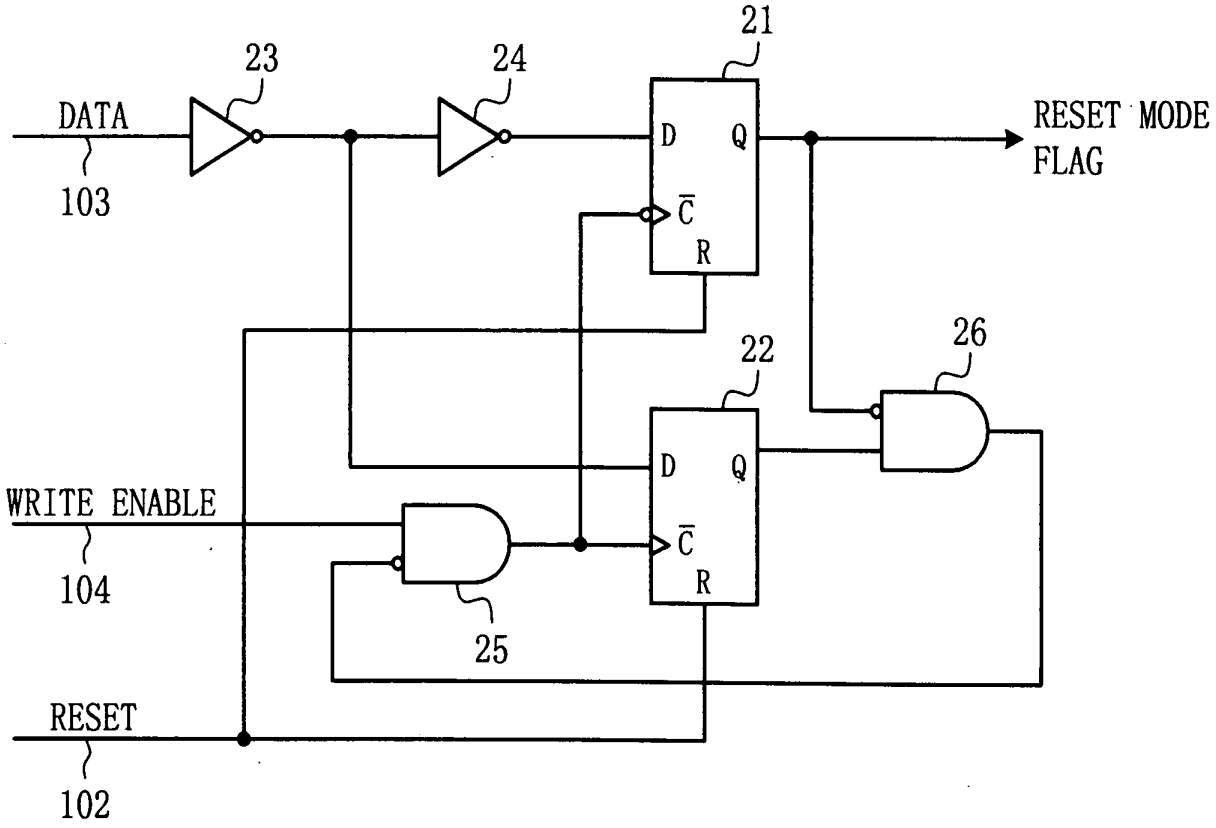
21
23
24
DATA
103
D
Q
RESET MODE
FLAG
C
R
26
22
D
Q
WRITE ENABLE
104
C
R
25
RESET
102

FIG. 6

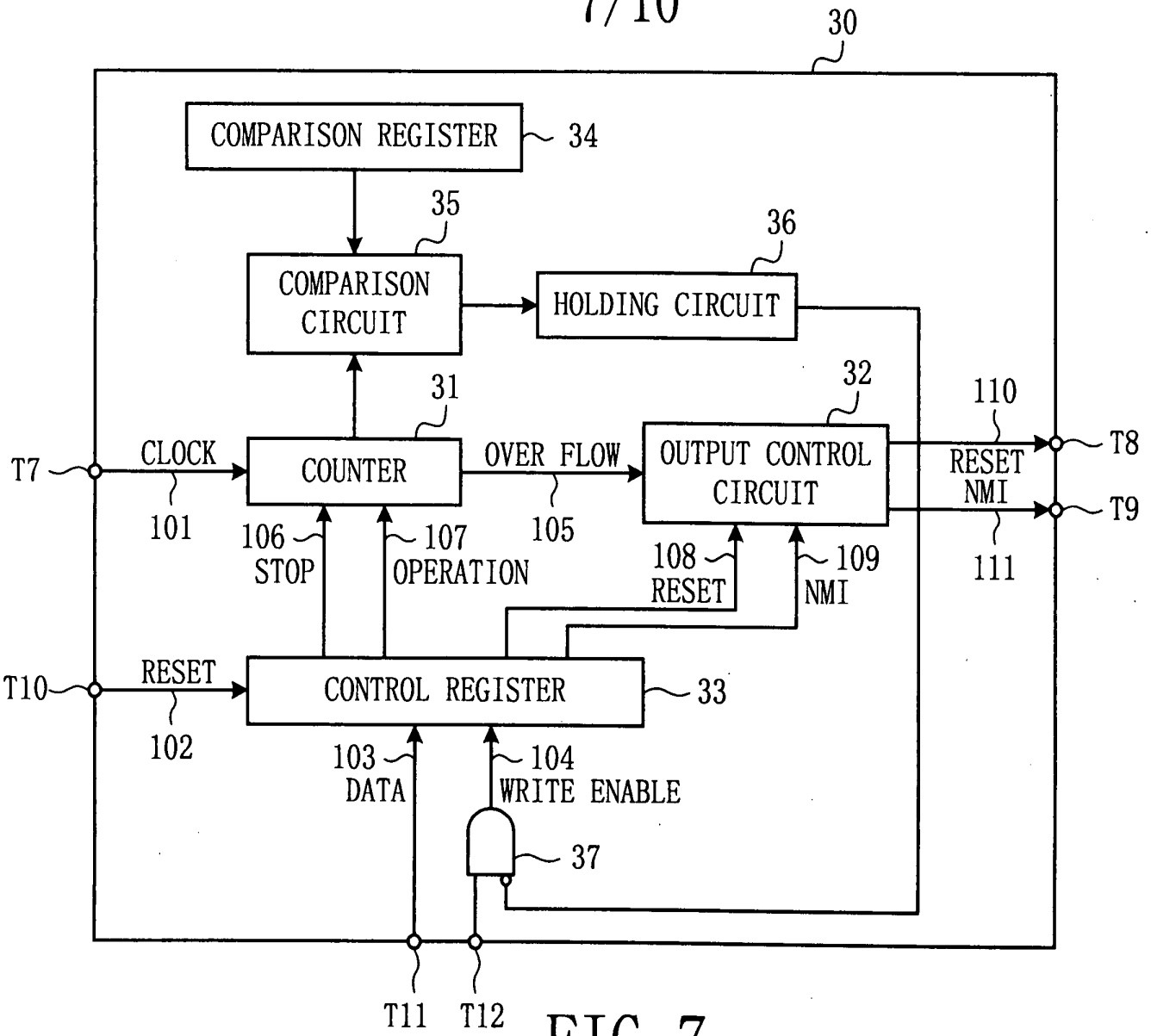
30
COMPARISON REGISTER
34
35
COMPARISON CIRCUIT
36
HOLDING CIRCUIT
31
32
110
T7
CLOCK
COUNTER
OVER FLOW
OUTPUT CONTROL CIRCUIT
RESET
NMI
T8
T9
101
106
STOP
107
OPERATION
105
108
RESET
109
NMI
111
T10
RESET
CONTROL REGISTER
33
102
103
DATA
104
WRITE ENABLE
37
T11
T12

FIG. 7

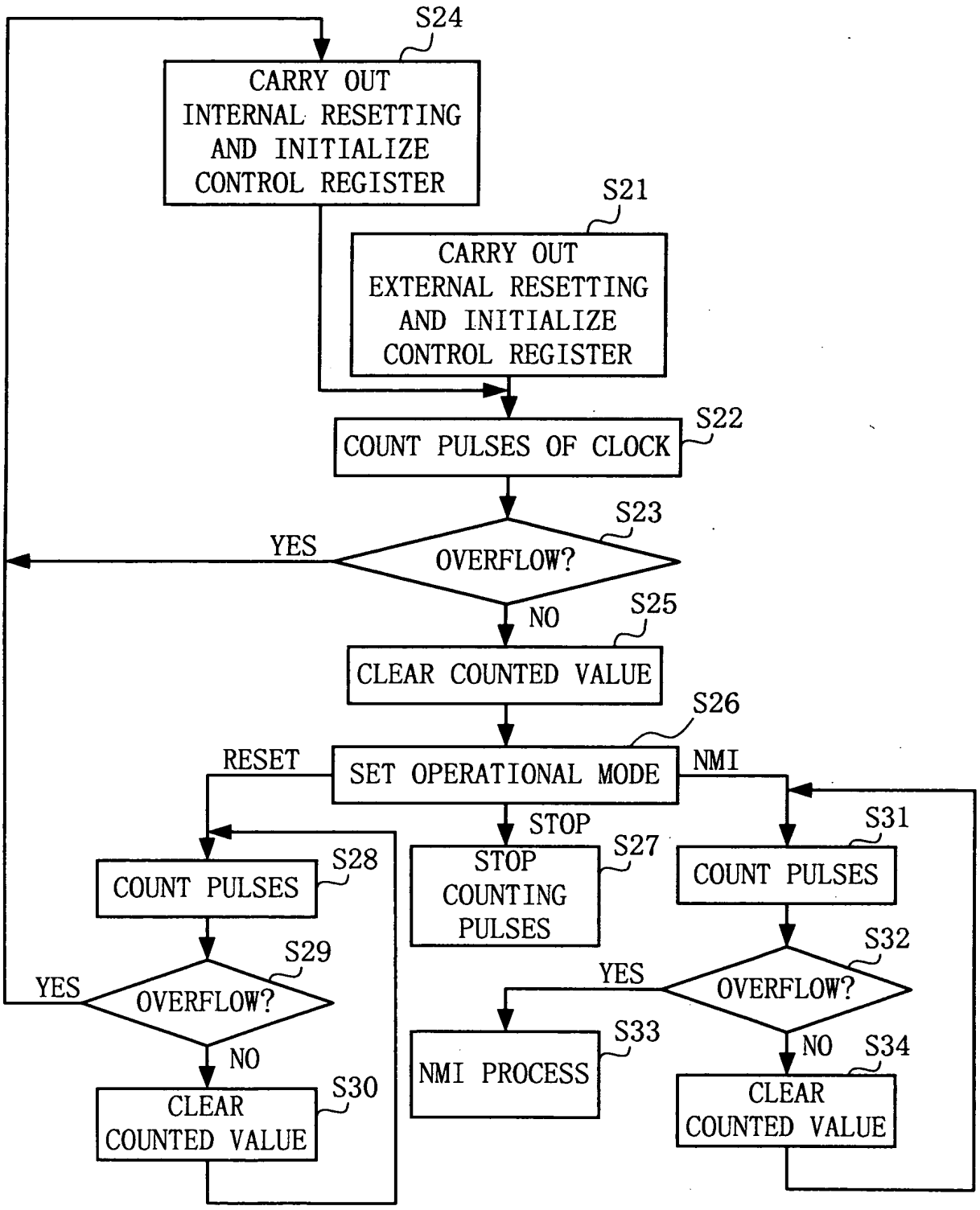
S24
CARRY OUT INTERNAL RESETTING AND INITIALIZE CONTROL REGISTER
S21
CARRY OUT EXTERNAL RESETTING AND INITIALIZE CONTROL REGISTER
S22
COUNT PULSES OF CLOCK
S23
YES
OVERFLOW?
NO
S25
CLEAR COUNTED VALUE
S26
RESET
SET OPERATIONAL MODE
NMI
STOP
S28
COUNT PULSES
S27
STOP COUNTING PULSES
S31
COUNT PULSES
S29
YES
OVERFLOW?
NO
S30
CLEAR COUNTED VALUE
S32
YES
OVERFLOW?
NO
S33
NMI PROCESS
S34
CLEAR COUNTED VALUE

FIG. 8

	ABNORMAL OPERATION	FACTOR
A	· TRANSISTOR(Tr) DOES NOT OPERATE · CLOCK FOR WDT IS NOT PROVIDED	· BREAKAGE OF POWER SOURCE LINE · BREAKAGE OF OSCILLATOR
B	· Tr OPERATES · CLOCK FOR WDT IS PROVIDED · SOFTWARE DOES NOT RUN	· ABNORMAL OPERATION IN CPU, ROM, RAM, ETC. (SUCH AS VOLTAGE DROP IN CPU)
C	· Tr OPERATES · CLOCK FOR WDT IS PROVIDED · SOFTWARE RUNS · TEMPORARY ABNORMALITY	· COMMON NOISE (E.G. IN POWER SOURCE) · ERROR IN SOFTWARE DESIGN (E.G. INDEFINED CONDITION)

FIG. 9

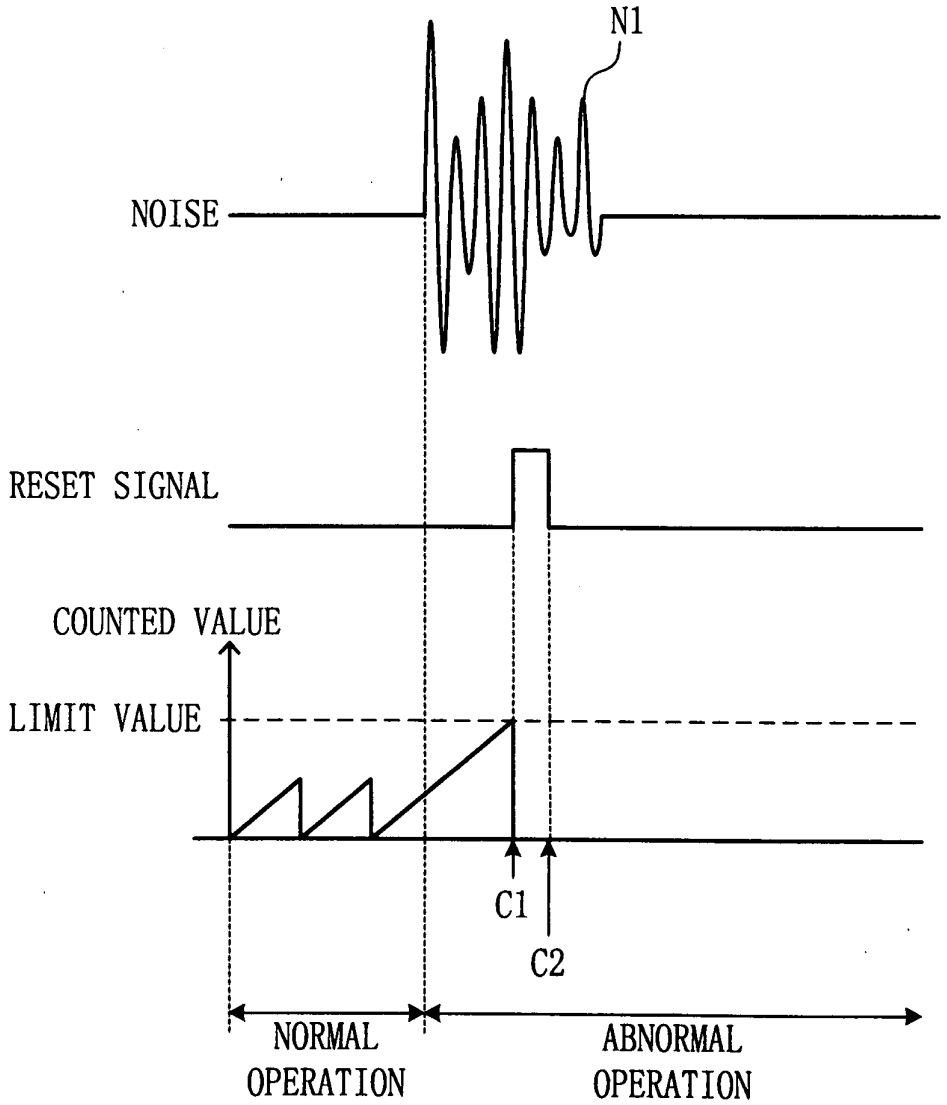
N1
NOISE
RESET SIGNAL
COUNTED VALUE
LIMIT VALUE
C1
C2
NORMAL OPERATION
ABNORMAL OPERATION

FIG. 10